Claims

What is claimed is:

1. A digital system, comprising:

a semaphore cell;

an interrupt generation circuit coupled to the semaphore cell;

a first processor coupled to the interrupt generation circuit; wherein

the semaphore cell is configured to have a first state and a second state, the first state of the semaphore cell indicating that a shared resource is available for access, and the second state of the semaphore cell indicating that the shared resource is unavailable for access, and

the interrupt generation circuit is configured to generate a first semaphore interrupt signal to the first processor when the semaphore cell changes from the second state to the first state and when the first processor need to access the shared resource.

2. The digital system of claim 1, wherein the interrupt generation circuit comprises a first semaphore interrupt enable cell coupled to the first processor and configured to have a third state and a fourth state, the third state of the first semaphore interrupt enable cell indicating that the first processor does not need to access the shared resource, and the fourth state of the first semaphore interrupt enable cell indicating that the first processor has read the semaphore cell and has determined that the semaphore cell is in the second state.

3. The digital system of claim 2, wherein the interrupt generation circuit further comprises a semaphore interrupt cell coupled to the semaphore cell and configured to have a fifth state and a sixth state, the sixth state of the semaphore interrupt cell indicating that the shared resource has just been made available for access.

4. The digital system of claim 3, wherein the interrupt generation circuit further comprises a first gate coupled to the semaphore interrupt cell, the first semaphore interrupt enable cell, and the first processor, the first gate being configured to generate the first semaphore interrupt signal to the first processor if the first semaphore interrupt enable cell is in the fourth state and the semaphore interrupt cell is in the sixth state.

5. The digital system of claim 4, wherein the first semaphore interrupt enable cell is further configured to change to the third state after the first semaphore interrupt signal is sent to the first processor.

6. The digital system of claim 4, wherein the semaphore interrupt cell is further configured to change to the fifth state after the first semaphore interrupt signal is sent to the first processor.

7. The digital system of claim 4, wherein the semaphore cell is configured to be in the second state after being read by any processor.

8. The digital system of claim 7, wherein the semaphore cell comprises a flip-flop coupled to the first processor via a control line, the control line being used for transmitting both read/write signals and data to be stored in the flip-flop.

9. The digital system of claim 4, wherein the interrupt generation circuit further comprises a second semaphore interrupt enable cell coupled to a second processor and configured to have a seventh state and an eighth state, the seventh state of the second semaphore interrupt enable cell indicating that the second processor does not need to access the shared resource, and the eighth state of the second semaphore interrupt enable cell indicating that the second processor reads the semaphore cell and finds that the semaphore cell is in the second state.

10. The digital system of claim 9, wherein the interrupt generation circuit further comprises a second gate coupled to the semaphore interrupt cell, the second semaphore interrupt enable cell, and the second processor, the second gate being configured to generate a second semaphore interrupt signal to the second processor if the second semaphore interrupt enable cell is in the eighth state and the semaphore interrupt cell is in the sixth state.

11. The digital system of claim 10, wherein the semaphore cell is configured to be in the second state after being read by any processor.

12. The digital system of claim 11, wherein the semaphore cell comprises a flip-flop coupled to the first and second processors via a control line, the control line being used for transmitting both read/write signals and data to be stored in the flip-flop.

13. A method of using semaphores to monitor shared resource accesses, the method comprising:

providing a semaphore cell configured to have a first state and a second state, the first state of the semaphore cell indicating that a shared resource is available for access, and the second state of the semaphore cell indicating that the shared resource is unavailable for access;

providing an interrupt generation circuit coupled to the semaphore cell;

providing a first processor coupled to the interrupt generation circuit; and

generating, with the interrupt generation circuit, a first semaphore interrupt signal to the first processor if the semaphore cell changes from the second state to the first state and if the first processor need to access the shared resource.

14. The method of claim 13, wherein the step of generating, with the interrupt generation circuit, a first semaphore interrupt signal to the first processor comprises providing a first semaphore interrupt enable cell coupled to the first processor and configured to have a third state and a fourth state, the third state of the first semaphore interrupt enable cell indicating that the first processor does not need to access the shared resource, and the fourth state of the first semaphore interrupt enable cell indicating that the first processor reads the semaphore cell and finds that the semaphore cell is in the second state.

15. The method of claim 14, wherein the step of generating, with the interrupt generation circuit, a first semaphore interrupt signal to the first processor further comprises providing a semaphore interrupt cell coupled to the semaphore cell and configured to have a fifth state and a sixth state, the sixth state of the semaphore interrupt cell indicating that the semaphore cell changes from the second state to the first state.

16. The method of claim 15, wherein the step of generating, with the interrupt generation circuit, a first semaphore interrupt signal to the first processor further comprises:

providing a first gate coupled to the semaphore interrupt cell, the first semaphore interrupt enable cell, and the first processor; and

generating, with the first gate, the first semaphore interrupt signal to the first processor if the first semaphore interrupt enable cell is in the fourth state and the semaphore interrupt cell is in the sixth state.

17. The method of claim 16, further comprising changing the first semaphore interrupt enable cell to the third state after the first semaphore interrupt signal is sent to the first processor.

18. The method of claim 16, further comprising changing the semaphore interrupt cell to the fifth state after the first semaphore interrupt signal is sent to the first processor.

19. The method of claim 16, wherein the step of providing the semaphore cell comprises providing a hardware semaphore cell.

20. The method of claim 19, wherein the step of providing a hardware semaphore cell comprises providing a flip-flop coupled to the first processor via a control line, the control line being used for transmitting both read/write signals and data to be stored in the flip-flop.

21. The method of claim 16, further comprising providing a second semaphore interrupt enable cell coupled to a second processor and configured to have a seventh state and an eighth state, the seventh state of the second semaphore interrupt enable cell indicating that the second processor does not need to access the shared resource, and the eighth state of the second semaphore interrupt enable cell indicating that the second processor reads the semaphore cell and finds that the semaphore cell is in the second state.

22. The method of claim 21, further comprising:

providing a second gate coupled to the semaphore interrupt cell, the second semaphore interrupt enable cell, and the second processor; and

generating, with the second gate, a second semaphore interrupt signal to the second processor if the second semaphore interrupt enable cell is in the eighth state and the semaphore interrupt cell is in the sixth state.